Neptune Vector Processor ASIC's

Non-function Units

- **Vector Register File - 20K, 8 used**
  2000 cells + RAM macros
  195 pins (140 in, 55 out)

- **Vector Merge/Microseq - 20K, 3 used**
  3200 cells - 1900 in VM reg
  247 pins (126 in, 121 out)

- **Input Staging - 10K, 2 used**
  700 cells
  122 pins (49 in, 73 out)

Function Units - preliminary

Approx 240 pins (160 in, 80 out)

- **Divide - Custom, 8 used**

- **Multiply - Custom, 4 used**

- **Float Add - Custom, 2 used**

- **Integer/Logical - 20K, 2 used**

C3 Vector Instruction Timing

PRELIMINARY

The x + y + z*VL notation means x clocks for initial overhead, y clocks until the first result is available afterwards, and z times vector length until the entire vector is complete. This lets you figure in chaining overlap in case the result is not used immediately (for which you can subtract y) or if one instruction chains into another (for which the second instruction may subract x since its initial overhead elapses while waiting for the first result from the first instruction).

inst	C3	C2	
ld.w	1 + 20 + vl/2	2 + 10 + vl	C3 if vs<2..0> == 4
ld.l	1 + 21 + vl	2 + 10 + vl	
st.w	1 + vl/2	2 + vl	Also stvi
st.l	1 + vl	2 + vl	
add.s	1 + 9 + vl/2	2 + 10 + vl	All add pipe & edits
add.d	1 + 10 + vl	2 + 10 + vl	
mul.s	1 + 9 + vl/2	2 + 12 + vl	
mul.d	1 + 11 + vl	2 + 12 + vl	
div.b	1 + 15 + vl/2	2 + 16 + vl	
div.h	1 + 23 + vl	2 + 24 + 1.5vl	
div.w	1 + 39 + 2vl	2 + 40 + 2.5vl	
div.l	1 + 71 + 4vl	2 + 72 + 4vl	
div.s	1 + 31 + 2vl	2 + 36 + 2.25vl	
div.d	1 + 60 + 4vl	2 + 64 + 4vl	

Operate from list (VM accelerate) adds 2 clocks to each instruction.
Operate under mask adds 4 to 6 clocks to loads.

Risks

Board area limitations

- Remove foreplane port support
- Remove add pipe functionality from multiply pipe
- Reduce quotient production rate by removing dividers
- Integrate some of Vector Dispatch

Custom function units